EyeQ TYPICAL VISION SYSTEM CONFIGURATIONS

Following is a typical configuration for an automotive vision sensor system:

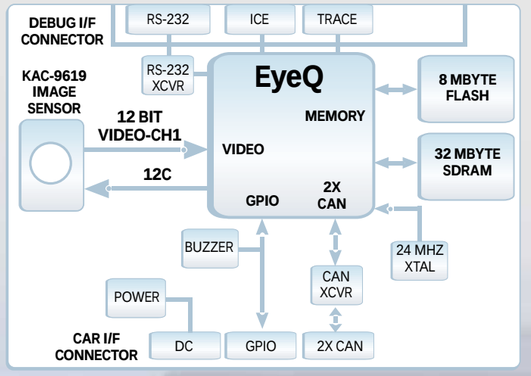

Figure 4. EyeQ Single Camera Module

A typical automotive vision sensor system uses an on board CMOS Image Sensor coupled with the Mobileye EyeQ device. The entire unit fits on a credit card size board.

EyeQ APPLICATIONS

A complete EyeQ based vision system including the camera, memories, data interfaces and power supply is compact enough to fit into the housing of a rear-view or side mirror, while providing the computing power for real time processing of the most complex driver assistance applications. The applications also support NIR and FIR night-vision cameras.

EyeQ offers a complete range of vision applications for driver assistance and for safety related applications. The applications are divided into four major types:

- Forward-looking applications
- Side-mirror applications
- Rear-looking applications
- In-cabin applications

Forward looking applications

Forward-looking applications include:

- Lane departure warning - provides warnings if lanes are inadvertently crossed and allows lane-keeping (active steering) and detection of driver drowsiness;
- Adaptive cruise control - allows automatic cruise-control and safe distance keeping under traffic congestion;
- Fusion with Radar for "Stop and Go" vehicle longitudinal control under urban conditions;
- Pre-crash - improving driving safety by detecting pedestrians and obstacles. These capabilities can be used in conjunction with pre-crash safety systems, or can provide an early warning to the driver, allowing preventive actions to reduce the injury to pedestrians and passengers and to reduce property damage.

Side mirror applications

Side mirror applications provide the driver with indications if lane change maneuvers are safe and the lanes are clear (Rear looking road analysis and Blind Spot detection). The system is compact enough to fit into a side mirror

Rear-looking applications

Rear looking cameras can provide rear collision warning and activate pre-crash safety mechanisms.

In-cabin applications

In-Cabin applications are intended to protect passengers from air-bag deployment in cases where the passengers may be hurt, and in order to meet new regulations regarding air-bag deployment, and include passenger classification (Adult, child, baby-seat, empty seat) as well as detection of out-of-position (passenger too close to air-bag). Additional driver assistance and safety applications are being developed, as well as other in-cabin convenience applications.

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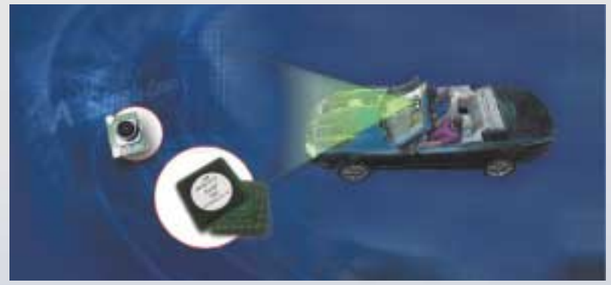
EyeQ™
Vision System on a Chip



HIGHLIGHTS:

- **110Mhz System Clock.**
- **Two ARM946E 32bit CPUs with DSP extensions.**
- **Four independent Vision Computing Engines (VCE)**
- **Eight channels DMA Controller.**
- **64bit width 288KB on-chip SRAM**
- **On chip peripherals, including: SDRAM, Flash Controller, I2C Master Controller two CAN Master/Slave, UART, I2C interfaces.**
- **Glue-less interfaces to two High Dynamic Range CMOS (HDRC) image sensors with I2C or SPI serial communication.**
- **Offers a unique solution for computationally intensive real-time visual recognition.**

INTRODUCTION

Mobileye's EyeQ™ System-on-Chip (SoC) offers a solution for computationally intensive real-time visual recognition and scene interpretation applications customized for use in intelligent vehicle systems. The chip architecture is designed to maximize cost performance by performing a fully-fledged application, such as a low-cost Adaptive Cruise Control using a single video source, on a single ultra low cost chip. The system detects vehicles, motorcycles, pedestrians and road markings to provide an intelligent driver assistance system. The system on chip technology translates to low cost in production. The EyeQ device meets automotive cabin qualification grade requirements.

The EyeQ chip is completely programmable to accommodate a wide range of visual processing applications beyond automotive applications.

EyeQ OVERVIEW & ARCHITECTURE

The EyeQ is manufactured using TSMC's CMOS 0.18-micron technology and runs at 110Mhz clock rate. This product is designed to comply with cabin-grade automotive qualification from -40ºC up to 85ºC.

In order to maximize total system cost performance, all peripheral circuits are integrated into the EyeQ, including dual CAN interfaces, UART, I2C controller, SDRAM controller, parallel I/O and two Video interface units.

The EyeQ architecture consists of two 32 bit RISC ARM946E CPUs, four independent Vision Computing Engines (VCE), multi channel DMA and several peripherals.

The four VCEs and the ARM946E Logic CPU perform in parallel all the intensive vision computations required by the applications such as tracking and pattern classification.

The Multi-Layer 4x4 Matrix block offers a high 64bit connectivity scheme that is needed for providing the required data bandwidth of the vision processing. The Multi-Layer matrix block routes the four master ports to the four slave ports and enables concurrent operation of up to four AHB buses. If there is a bus contention on a slave port, the Multi-Layer AHB matrix block decides on the winning AHB master according to the priority scheme.

All the VCEs work in parallel, read their tasks from internal tasks queues and retrieve the necessary images from the high-speed 64bit width 288Kbyte on-chip SRAM.
A separate 32-bit low bandwidth Application Peripheral Bus (APB) is provided to connect all of the various peripherals such as the CAN drivers.

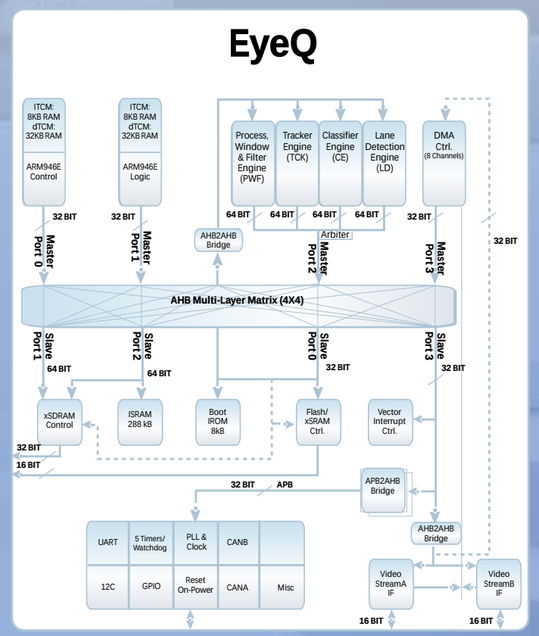


Figure 1. EyeQ Block Diagram

ARM946E Control & Logic CPUs

An ARM946E Control CPU manages all the resources on EyeQ and implements the high-level algorithmic tasks. It is located on the Master Port0 of the Multi Layer AHB matrix unit.
An additional ARM946E Logic CPU implements parts of the algorithm that are control-oriented code. It is located on Master Port1 of the Multi Layer AHB matrix unit.

Each ARM946E includes:

- ARM946E CPU with DSP instructions
- 8Kbyte Instruction and Data Caches
- 32Kbyte Tight Couple Memory (TCM) for Data and 8Kbyte TCM for instructions

Vision Computing Engines (VCE):

The four VCE modules share the 64 bit Master Port2 and Slave Port0 on the Multi Layer (see figure 2). In order to enable the VCEs to process the vision tasks concurrently, each one is furnished with:

- DMA channels which are configured by the VCE according to the task being processed and transfer the Image data between the off-chip or on-chip memories and their ACE local memories.
- Local memory to hold the image data required by the task, thereby reducing the load on the Multi Layer buses.
- A vision core that performs the specific vision algorithms.
- Shared Memory holding up to eight tasks. This memory is also used to store the vision task results. The ARM946E Control is activated by the multi channel DMA which removes the tasks' results from the tasks queue and reloads it with new tasks. This is done without interfering the ARM946E Control.

Vision Computing Engines:

- Classifier Engine (CE):
  - Image scaling & preprocessing.
  - Image pattern classifier.
- Tracker Engine (TCK):
  - Image warping.
  - Image tracking.
- Lane Detection Engine (LD):
  - Lane marks detection.
  - Road Geometry detection.
- Preprocessing, Window and Filter Engine (PWF):
  - Image convolver.
  - Image pyramid creation.
  - Edge detection.
  - Image filters.
  - Image histogram.

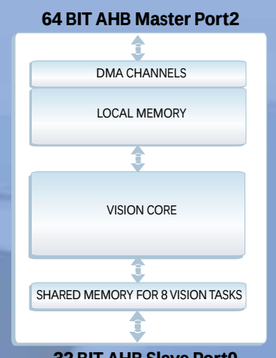


Figure 2. VCE Block Diagram

DMA Controller:

The eight-channel DMA Controller is located on Master Port3 of the multi Layer Matrix block. The DMA Controller is programmed by the ARM946E Control CPU to support the video stream capture via the Video Interfaces block and for on-chip and off chip general data transactions. The DMA Controller main features are:

- Supports Memory to memory, Peripheral to memory, and Peripheral to peripheral transfers
- Up to 16 peripheral DMA requests
- 8 DMA channels, each channel supports a unidirectional transfer
- Scatter or Gather DMA is supported through the use of linked lists
- Two AHB masters for transferring data
- 32 bit AHB bus width

AHB 64 bit Multi Layer 4x4 Matrix Block:

The AHB Multi-Layer 4x4 Matrix block enables a high connectivity scheme that is required to provide the data bandwidth of the vision processing. The AHB Multi-Layer Matrix routes the four Master Ports to the four Slave Ports and enables concurrently up to four AHB paths with the following properties:

- If there is a contention on a Slave Port, the Multi-Layer decides on the Master Port according to the priority scheme.
- Supports 64bit and 32bit wide interconnection scheme based on the AHB protocol.
- Enables parallel routing, up to four paths, between four Master Ports and four Slave Ports.

Two Video Interfaces:

The Video Interface supports the capturing of two high dynamic range (90-120dB) video streams usually of 640x480 image resolution each. The Video Interface supports Slave and Master modes. The interface between the Image Sensor and EyeQ is without any glue. A typical Image Sensor is the Kodak 12 bit KAC-9619. The Video Interface gets either color or monochrome high dynamic range (90-120dB) image video streams. The Video Interface gets the video stream, runs the pixel pre-processing and stores the 8bit images in the two FIFOs. EyeQ configures the Image Sensor via the I2C Interface or GPIO.

- Supports two VGA color image resolution video streams
- Twelve bits Glue-less interface to high dynamic Image sensor
- Color Video Bayer De-mosaic mechanism.
- Twelve bits to eight bits pixel compression with highly configurable 256 points Gamma curve approximation.

Memory support:

EyeQ supports several off-chip and on-chip memory units:

- On-chip 288KByte 64 bits data width fast memory located on the Multi Layer Matrix block Slave Port2.
- On-chip 8KByte for bootstrap code locates on the Multi Layer Matrix block Slave Port0.
- 32 bit external SDRAM controller located on the Multi Layer Matrix block Slave Port1
- 16 bit external Flash and SRAM controller located on the Multi Layer Matrix block Slave Port0

Other peripherals:

- Vector Interrupt Controller:
  - Supports 32 interrupt sources
  - Supports 16 interrupt vectors
- Serial Interfaces:
  - UART controller
  - 2 x CAN controller
  - I2C Controller
- Others:
  - 16 bit GPIO
  - Five Timers, includes Watch-Dog.
  - PLL
  - Power On Reset
  - Trace Port and 3KB Trace buffer

EyeQ PINOUT DESCRIPTION

The EyeQ is packaged in a 292balls Heat Sink Ball Grid Array (HSBGA).

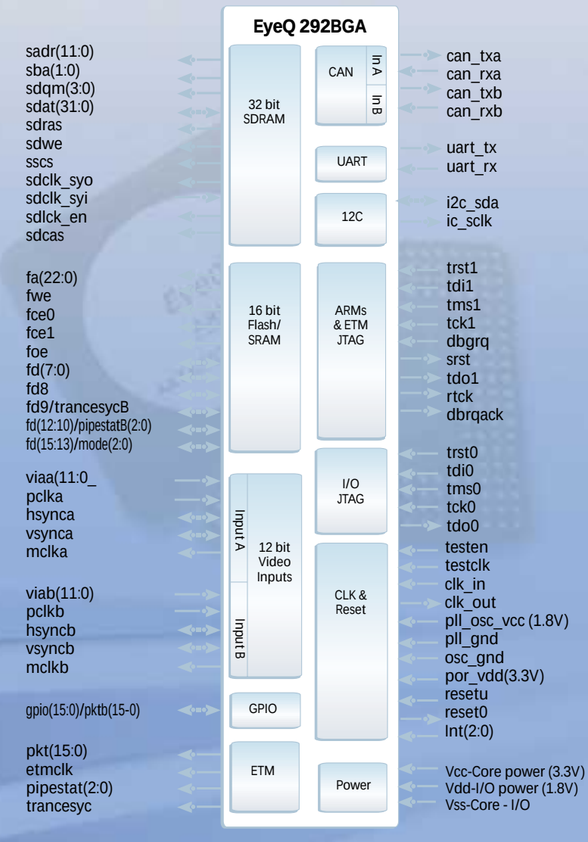


Figure 3. EyeQ 292 HSBGA package